AMENDMENTS TO THE CLAIMS

Please replace the claims, including all prior versions, with the listing of claims found below.

Listing of Claims:

1. (Previously presented) A circuit comprising:

a first switching element coupled to a first terminal and a second terminal;

a second switching element coupled to the first terminal; and

a capacitor coupled between the second switching element and a ground or reference voltage.

2. (Previously presented) The circuit of claim 1, further comprising:

a first clock signal to switch the first switching element between high and low; and

a second clock signal to switch the second switching element between high and low.

3. (Previously presented) The circuit of claim 2, wherein the second clock signal is the phase-shifted complementary signal of the first clock signal.

4. (Currently amended) The circuit of claim 1, wherein

the circuit operates to ~~reduce charge injection and clock feed-through error voltage~~ substantially null and cancel the charge injection charges and clock feed-through charges, respectively, by absorbing the charge injection charges into the capacitor and by generating a compensation signal.

5. (Previously presented) The circuit of claim 4, wherein the circuit replaces a switching element in a switched network.

6. (Previously presented) A switching element, comprising:

a circuit including a first switching element coupled to a first terminal and a second terminal, a second switching element coupled to the first terminal, and a capacitor coupled between the second switching element and a ground or reference voltage.

7. (Currently amended) The switching element of claim 6, wherein the circuit substantially nulls a charge injection charges by absorbing the charge injection charges into the capacitor and canceling the feed-through charges by generating a compensation signal with opposite polarity at the first terminal.

8. (Previously presented) The switching element of claim 7, wherein the circuit replaces another switching element in the switched network.

9. (Currently amended) The switching element of claim 8, wherein the another switching element is connected to a node in the switched network where there is a charge injection charges or a clock feed-through charges.

10. (Currently amended) A method of nulling a charge injection and a clock feed-through charges ~~error voltage~~ in a switched network, comprising:

replacing at least one switching element in the switched network with a nulling circuit, the nulling circuit nulling the charge injection charges by absorbing the charge injection charges in a capacitor.

11. (Currently amended) The method of claim 10, further comprising:

generating a compensation signal such that the clock feed-through charges ~~error voltage~~ has been removed.

12. (Currently amended) A method of nulling a charge, comprising:

switching a first switching element to off by turning a first clock signal to low, causing a charge injection charges and a clock feed-through charges to flow into a first node; and

switching a second switching element to on by turning a second clock signal to high, nulling the charge injection charges and clock feed-through charges as a result of absorbing the charge injection charges into a capacitor and generating a compensation signal with opposite polarities, respectively.

13. (Currently amended) A method of nulling a charge injection in a switched network, comprising:

a first switching element causing charge injection charges and clock feed-through charges to flow into a node; and

a second switching element nulling the charge injection charges that flow into the node by absorbing the charges in a capacitor and canceling the feed-through charges by a compensation signal with opposite polarity.

14. (Currently amended) The method of claim 13, wherein

the flow of charges into the node ~~injecting~~ occurs as a result of providing a first clock signal to a first switch such that the first switch is turned off, and

the nulling occurs as a result of providing a second clock signal to a second switch such that the second switch is turned on, resulting in the compensation signal.

15. (Previously presented) A circuit comprising:

a first switching element coupled to a first node and a second node;

a second switching element coupled to the first node;

a third switching element coupled to the second node;

a first capacitor coupled between the second switching element and a ground or reference voltage; and

a second capacitor coupled between the third switching element and the ground or reference voltage.

16. (Previously presented) The circuit of claim 15, further comprising:

a first clock signal to switch the first switching element between high and low; and

a second clock signal to switch the second and third switching elements between high and low.

17. (Previously presented) The circuit of claim 16, wherein the second clock signal is the phase-shifted complementary signal of the first clock signal.

18. (Currently amended) The circuit of claim 15, wherein

the circuit operates to ~~reduce the charge injection and clock feed-through error voltage~~ substantially null and cancel the charge injection charges and clock feed-through charges, respectively, by absorbing the charge injection charges into the first and second capacitors and by generating a compensation signal on the first and second nodes.

19. (Previously presented) The circuit of claim 18, wherein the circuit replaces a switching element in a switched network.

20. (Previously presented) A switching element, comprising:

a circuit including a first switching element coupled to a first node and a second node a second switching element coupled to the first node, a third switching element coupled to the second node, and a first capacitor coupled between the second switching element and a ground or reference voltage, and a second capacitor coupled between the third switching element and the ground or reference voltage.

21. (Currently amended) The switching element of claim 20, wherein the circuit substantially nulls a charge injection charges by absorbing the charge injection charges into the first and second capacitors and canceling the feed-through charges by generating a compensation signal with opposite polarity at the first and second nodes.

22. (Previously presented) The switching element of claim 21, wherein the circuit replaces another switching element in a switched network.

23. (Currently amended) The switching element of claim 22, wherein the another switching element is connected to a node in the switched network where there is a charge injection charges or a clock feed-through charges ~~error voltage is high~~.

24. (Currently amended) A method of nulling a charge injection charges and a clock feed-through charges ~~error voltage~~ in a switched network, comprising:

replacing at least one switching element in the switched network with a nulling circuit, the nulling circuit nulling the charge injection charges by absorbing the charge injection charges in a first capacitor and a second capacitor.

25. (Currently amended) The method of claim 24, further comprising:

generating a compensation signal on a first node and a second node such that the clock feed-through charges ~~error voltage~~ has been removed.

26. (Currently amended) A method of nulling a charge, comprising:

switching a first switching element to off by turning a first clock signal to low, causing a charge injection charges and a clock feed-through charges to flow into a first node and a second node; and

switching a second switching element and a third switching element to on by turning a second clock signal to high, nulling the charge injection charges and clock feed-through charges as a result of absorbing the charge injection charges into a first capacitor and a second capacitor and generating a compensation signal with opposite polarities. respectively.

27. (Currently amended) A method of nulling a charge injection in a switched network, comprising:

a first switching element causing charge injection charges and clock feed-through charges to flow into a first node and a second node; and

a second switching element and a third switching element nulling the charge injection charges that flow into the first and second nodes respectively by absorbing the charges in a first capacitor and a second capacitor and canceling the feed-through charges by a compensation signal with opposite polarity on the first and second nodes.

28. (Currently amended) The method of claim 27, wherein

the flow of charges into the first and second node ~~injecting~~ occurs as a result of providing a first clock signal to a first switch such that the first switch is turned off, and

the nulling occurs as a result of providing a second clock signal to a second switch and a third switch such that the second and third switches are turned on, resulting in the compensation signal on the first and second nodes.